

brought in contact with either one of the IC chip 1 and the board 4 is mixed with a smaller amount of inorganic filler than the other portion 701 or the layer 6y or with no inorganic filler 6f, the reduction in the adhesive strength
5 due to the large amount of inorganic filler can be prevented.

A variety of modification examples of this twenty-ninth embodiment will be described below.

First, as a first modification example, as shown
10 in Fig. 63C, Fig. 64C and Fig. 67A, the insulating resin layers 6 and 306b can be constructed so that the portion 700 brought in contact with both the IC chip 1 and the board 4 is mixed with a smaller amount of inorganic filler than the other portion 701 or with no inorganic filler 6f.
15 Also, in this case, it is acceptable to gradually vary the amount of inorganic filler without definitely distinguishing the portion 700 brought in contact with both the IC chip 1 and the board 4 from the other portion 701 as shown in Fig. 63C or to definitely distinguish them from
20 each other as shown in Fig. 64C and Fig. 67A. That is, in Fig. 64C and Fig. 67A, it is acceptable to make the insulating resin layers 6 and 306b have a multilayer structure further provided with a third resin layer 6z that is located on the opposite side of the first resin layer 6x
25 with respect to the second resin layer 6y and is

constructed of the insulating resin mixed with a smaller amount of inorganic filler than the first resin layer 6x or no inorganic filler 6f and bring the first resin layer 6x and the third resin layer 6z in contact with the IC chip 1 and the board 4, respectively.

Furthermore, as another modification example, it is acceptable to mix the portion 700 brought in contact with the IC chip 1 or the board 4 or both of them with the inorganic filler by less than 20 wt% or with no inorganic filler 6f and mix the other portion 701 with the inorganic filler by not less than 20 wt%. In this case, it is acceptable to gradually vary the amount of inorganic filler without definitely distinguishing the portion 700 brought in contact with the IC chip 1 or the board 4 or both of them from the other portion 701 as shown in Figs. 63A, 63B and 63C or to definitely distinguish them from each other as shown in Figs. 64A, 64B and 64C, Fig. 65, Fig. 66 and Fig. 67A. That is, it is possible to mix the first resin layer 6x or the first resin layer 6x and the third resin layer 6z with the inorganic filler by less than 20 wt% or with no inorganic filler 6f and mix the second resin layer 6y with the inorganic filler by not less than 20 wt%.

As a concrete example, assuming that the insulating resin 306m is provided by thermosetting epoxy resin, then the second resin layer 6y occupies 50 wt% in

the case of a ceramic board or 20 wt% in the case of a glass epoxy board. As an example, the first resin layer 6x or the third resin layer 6z or both of them are made to have a thickness of 15 μm , while the second resin layer 6y 5 is made to have a thickness of 40 to 60 μm . The thickness of the insulating resin layers 6 and 306b is made to have a dimension larger than the gap dimension obtained after the bonding of the IC chip 1 to the board 4, so that the space between the IC chip 1 and the board 4 is completely filled 10 with the layer at the time of bonding of the IC chip 1 to the board 4, further ensuring the connection.

As another modification example, it is acceptable to reverse the loadings of the inorganic filler with respect to the modification example shown in Fig. 63C, Fig. 15 64C and Fig. 67A. That is, as shown in Fig. 63D, it is acceptable that a middle portion 702 of the portion 703 that belongs to the insulating resin layers 6 and 306b and is brought in contact with both the IC chip 1 and the board 4 is mixed with a smaller amount of inorganic filler than 20 the portion 703 brought in contact with both the IC chip 1 and the board 4 or with no inorganic filler 6f. Also in this case, it is acceptable to gradually vary the amount of inorganic filler without definitely distinguishing the portion 703 brought in contact with both the IC chip 1 and 25 the board 4 from the middle portion 702 or to definitely